FIG. 1A

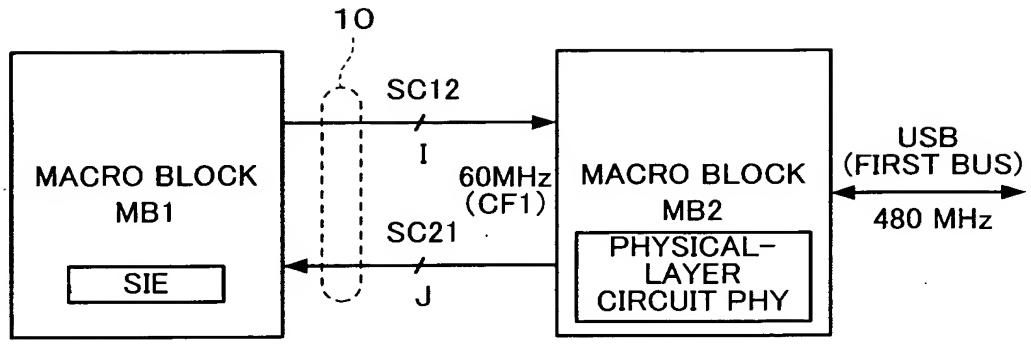

10
SC12
I
60MHz
(CF1)
SC21
J
MACRO BLOCK
MB1
SIE
MACRO BLOCK
MB2
PHYSICAL-
LAYER
CIRCUIT PHY
USB
(FIRST BUS)
480 MHz

FIG. 1B

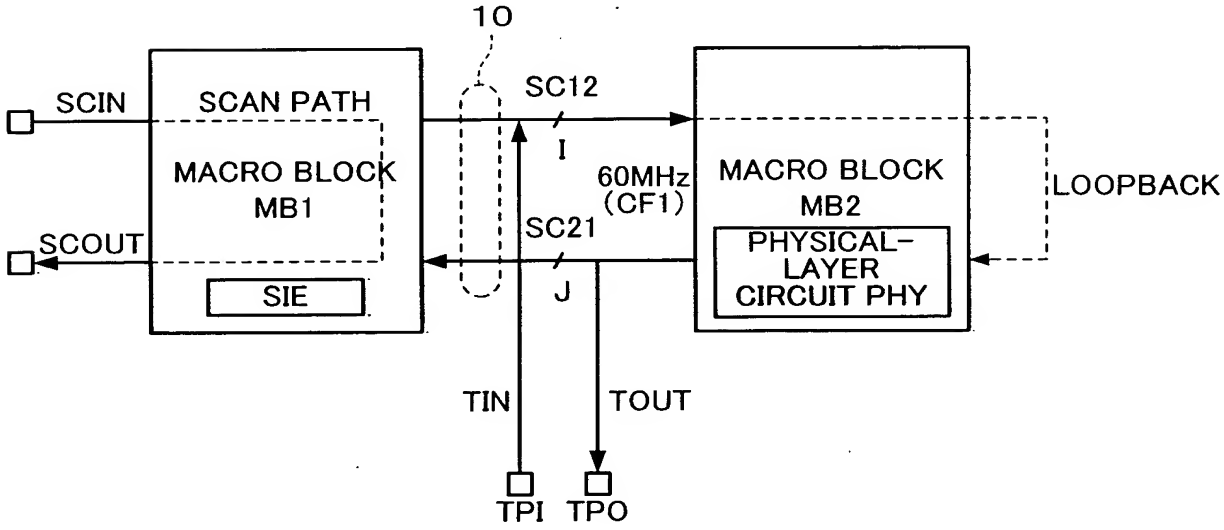

10
SCIN
SCAN PATH
MACRO BLOCK
MB1
SCOUT
SIE
SC12
I
60MHz
(CF1)
SC21
J
MACRO BLOCK
MB2
PHYSICAL-
LAYER
CIRCUIT PHY
LOOPBACK
TIN
TOUT
TPI
TPO

FIG. 2

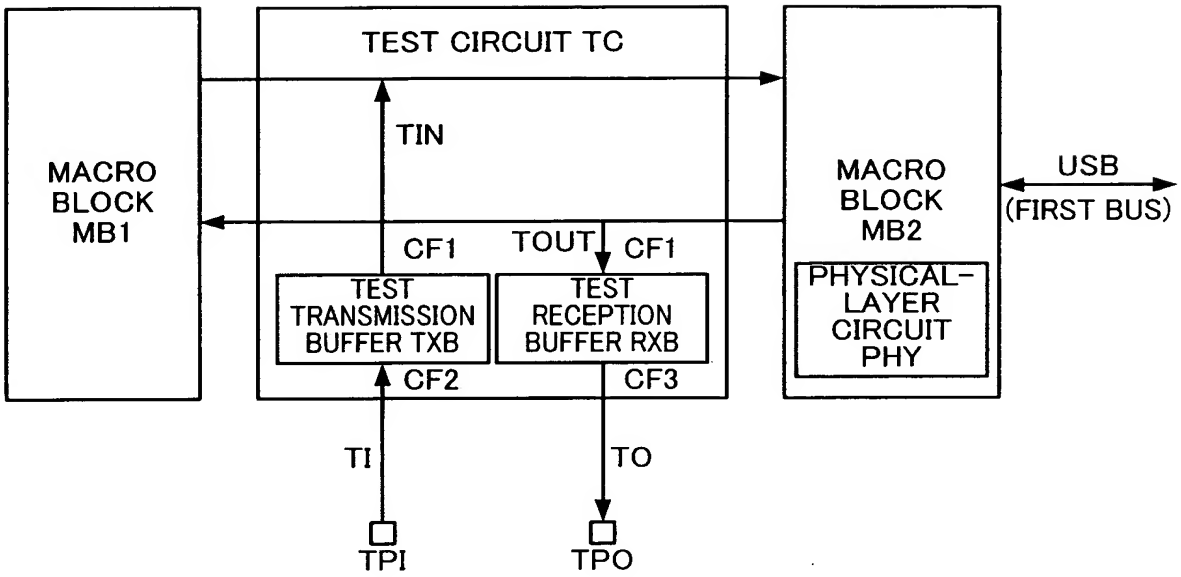

TEST CIRCUIT TC
MACRO BLOCK MB1
TIN
MACRO BLOCK MB2
USB (FIRST BUS)
CF1
TOUT
CF1
TEST TRANSMISSION BUFFER TXB
TEST RECEPTION BUFFER RXB
PHYSICAL-LAYER CIRCUIT PHY
CF2
CF3
TI
TO
TPI
TPO

FIG. 3A

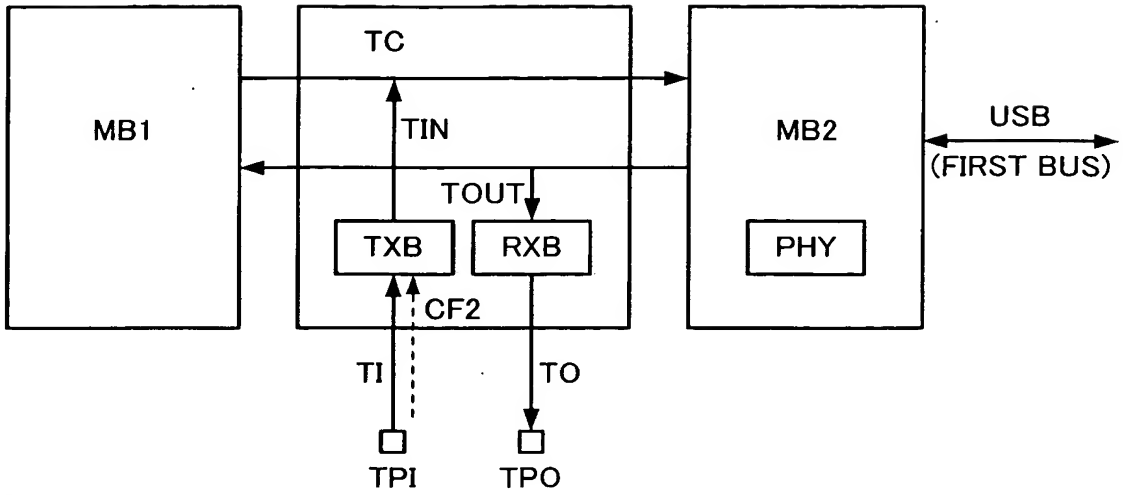


FIG. 3B

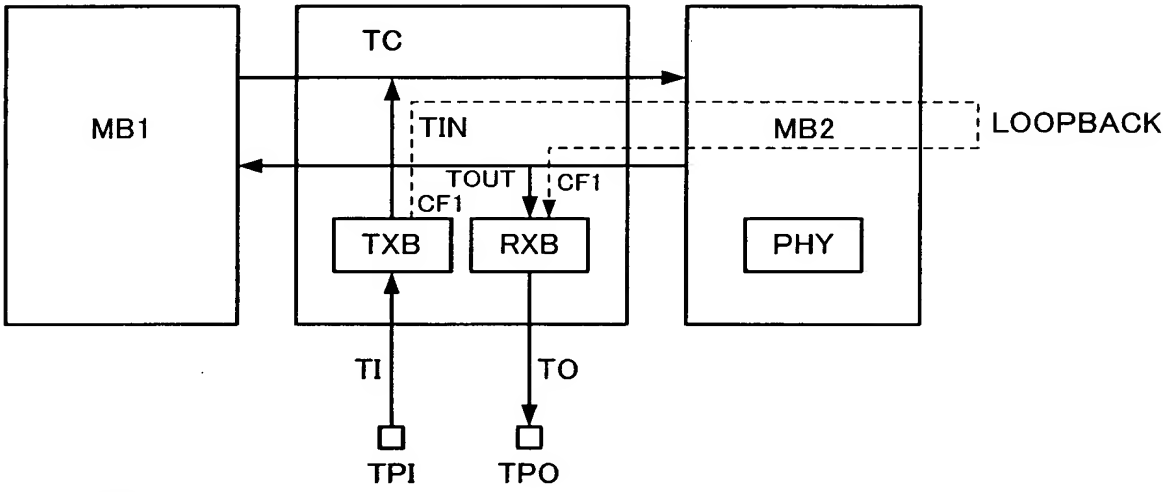


FIG. 3C

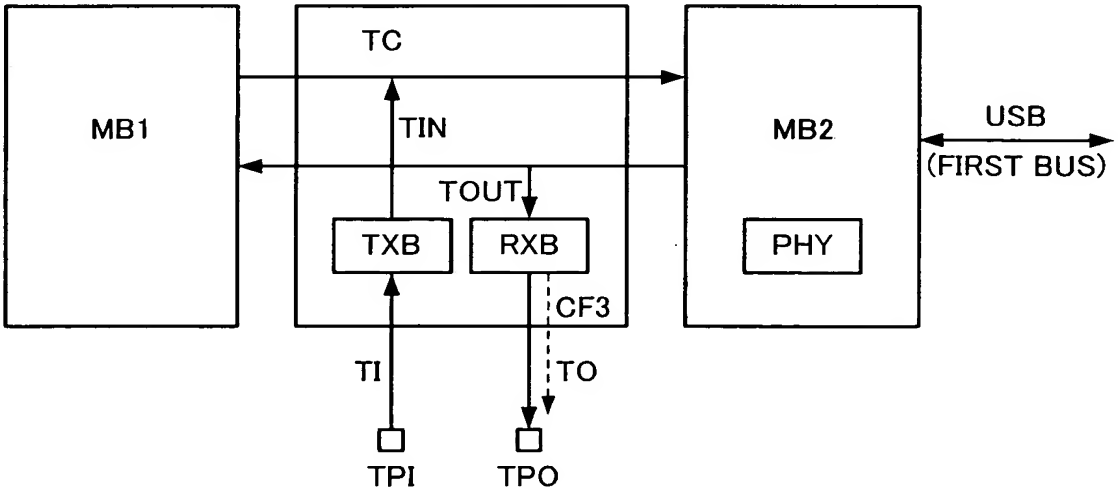


FIG. 4

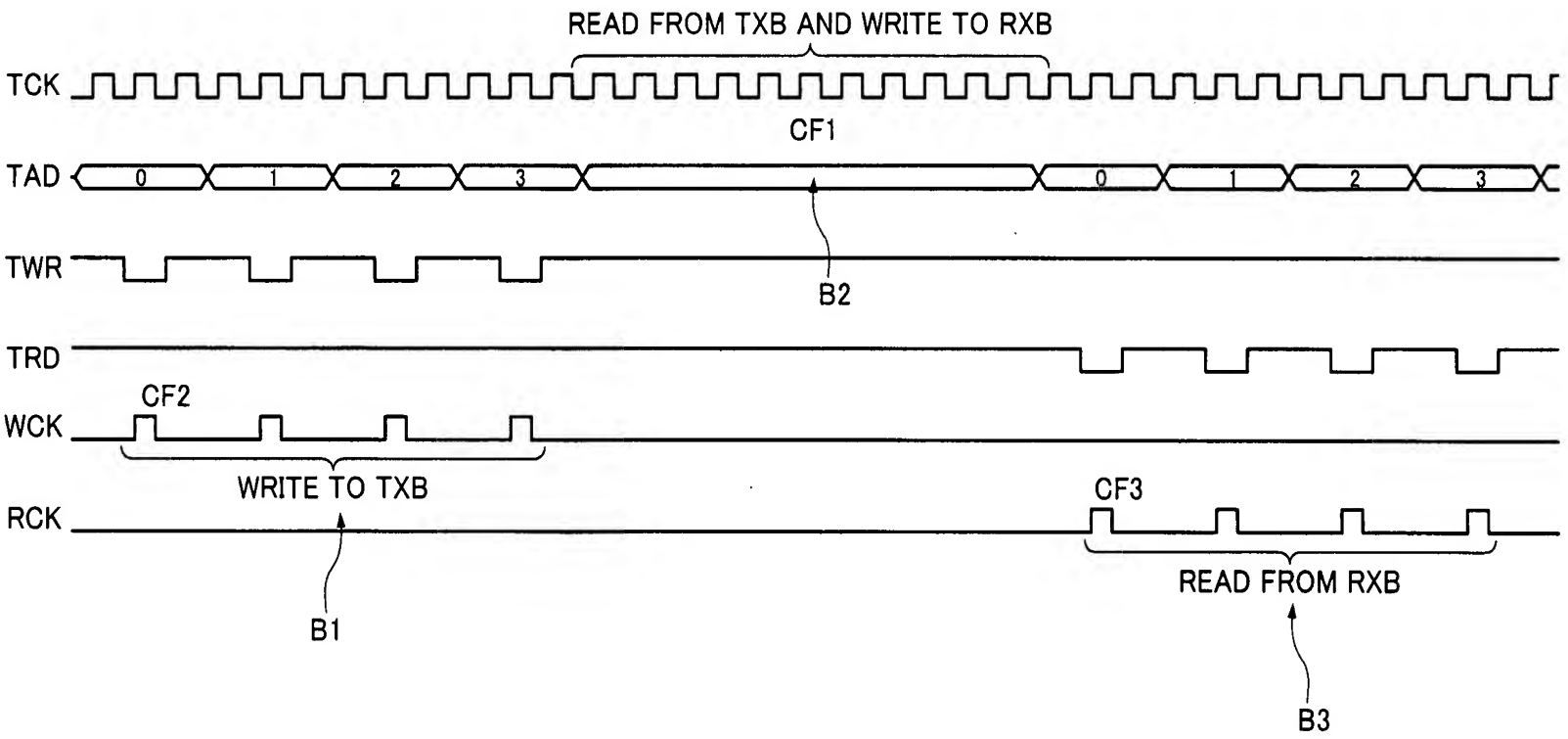

READ FROM TXB AND WRITE TO RXB
TCK
CF1
TAD
0
1
2
3
0
1
2
3
TWR
B2
TRD
CF2
WCK
WRITE TO TXB
CF3
RCK
READ FROM RXB
B1
B3

FIG. 5

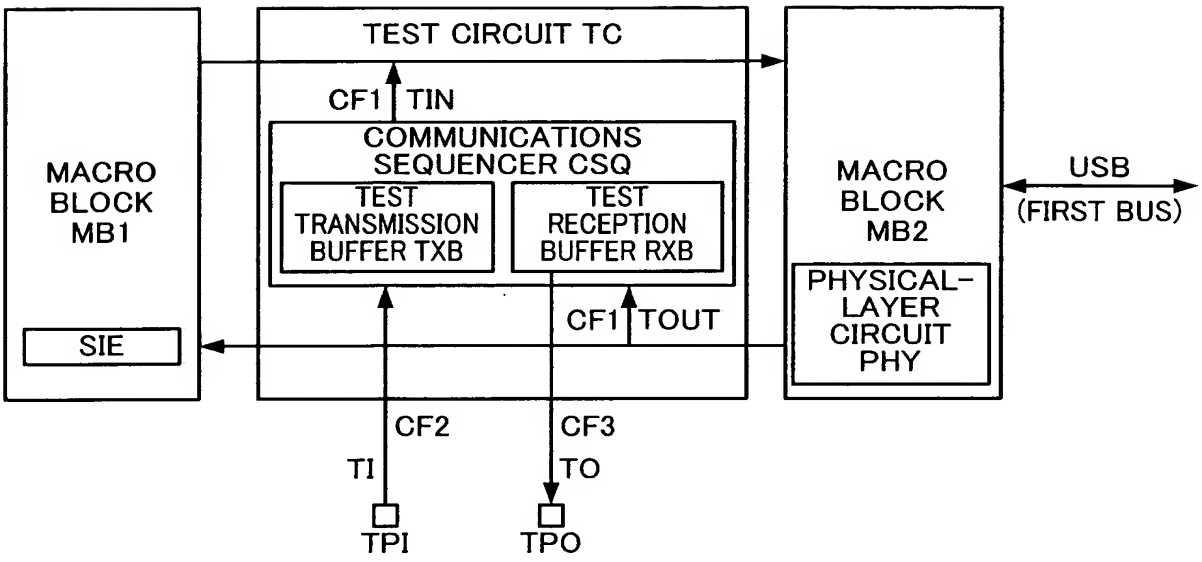

TEST CIRCUIT TC
CF1
TIN
COMMUNICATIONS SEQUENCER CSQ
TEST TRANSMISSION BUFFER TXB
TEST RECEPTION BUFFER RXB
MACRO BLOCK MB1
SIE
CF1
TOUT
MACRO BLOCK MB2
PHYSICAL-LAYER CIRCUIT PHY
USB
(FIRST BUS)
CF2
TI
CF3
TO
TPI
TPO

FIG. 6

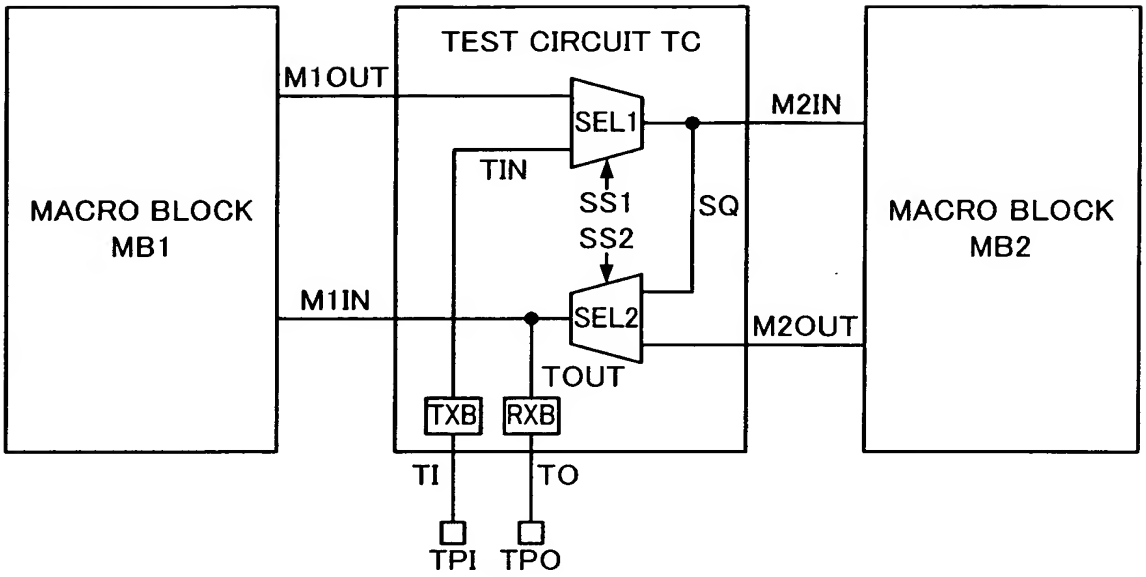

TEST CIRCUIT TC
M1OUT
SEL1
M2IN
TIN
SS1
SS2
SQ
MACRO BLOCK
MB1
MACRO BLOCK
MB2
M1IN
SEL2
M2OUT
TOUT
TXB
RXB
TI
TO
TPI
TPO

FIG. 7A FIRST TEST MODE

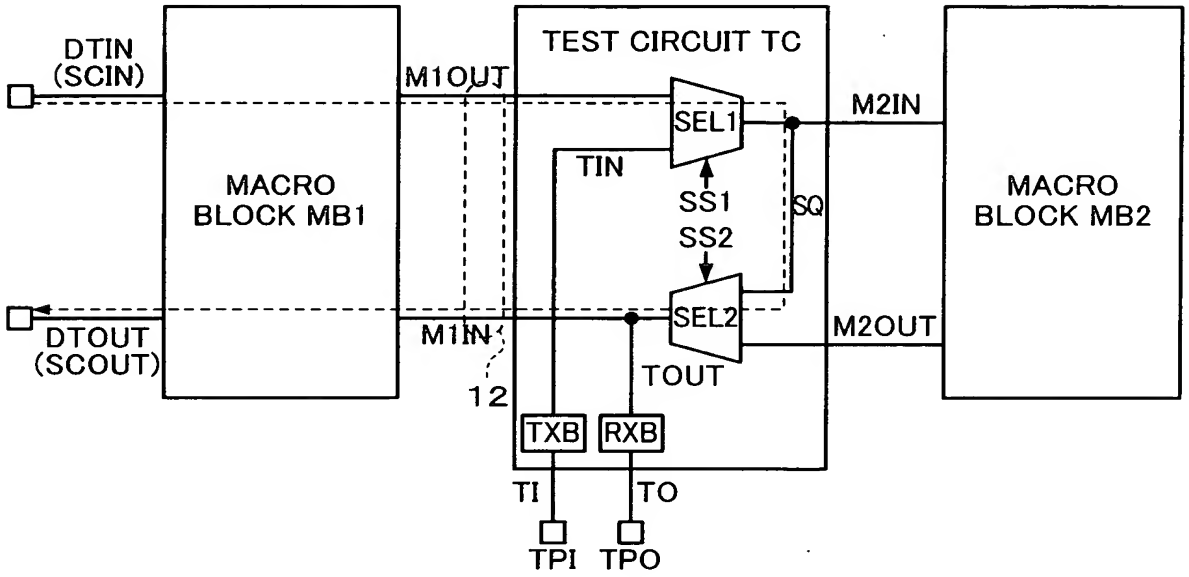


FIG. 7B SECOND TEST MODE

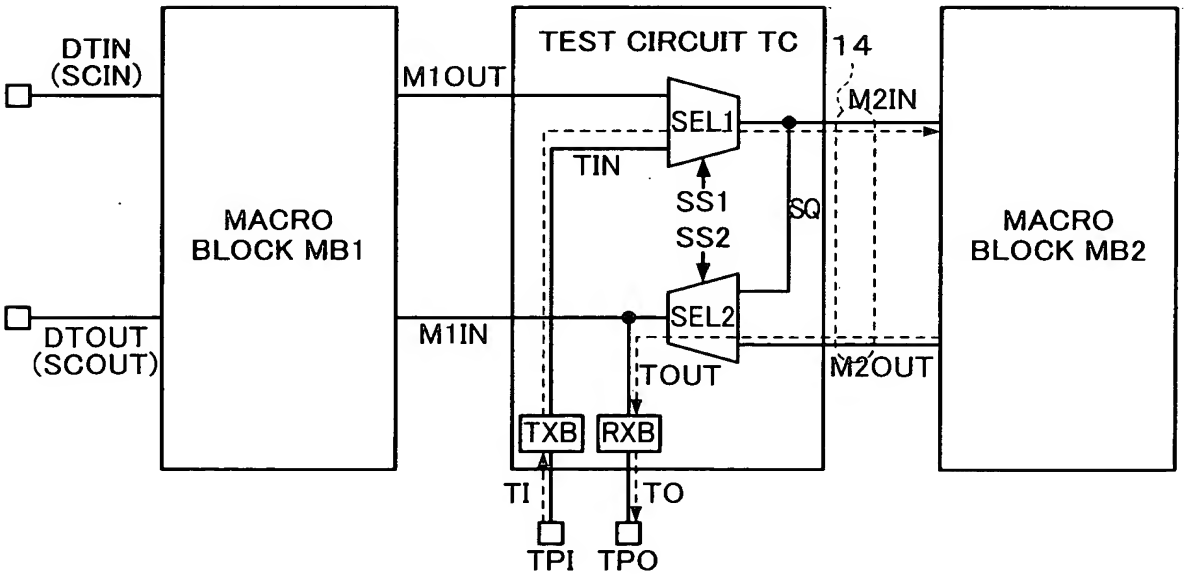


FIG. 8

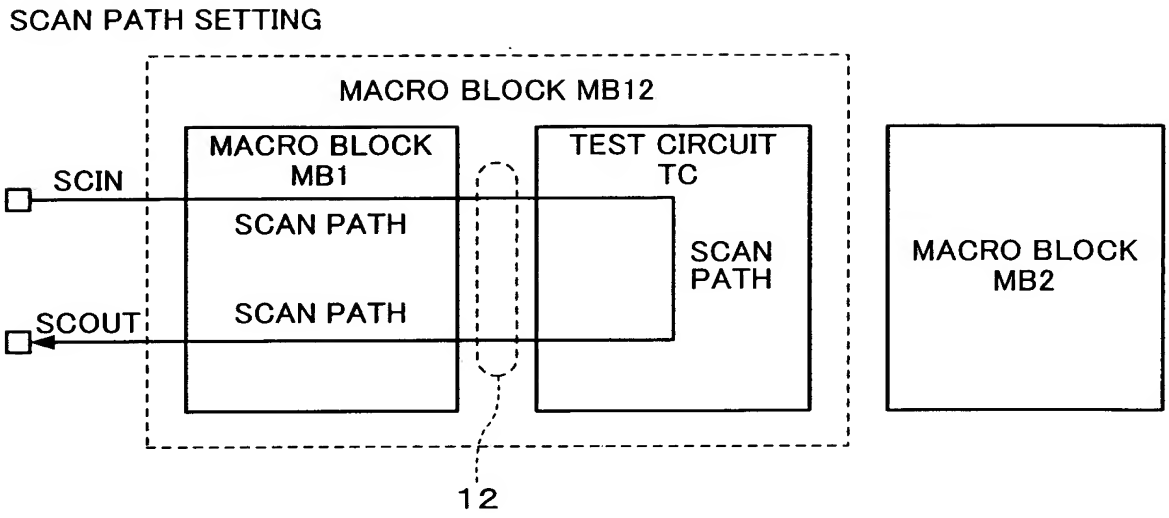

SCAN PATH SETTING
MACRO BLOCK MB12
MACRO BLOCK MB1
TEST CIRCUIT TC
SCIN
SCAN PATH
SCAN PATH
SCAN PATH
SCOUT
MACRO BLOCK MB2
12

FIG. 9A

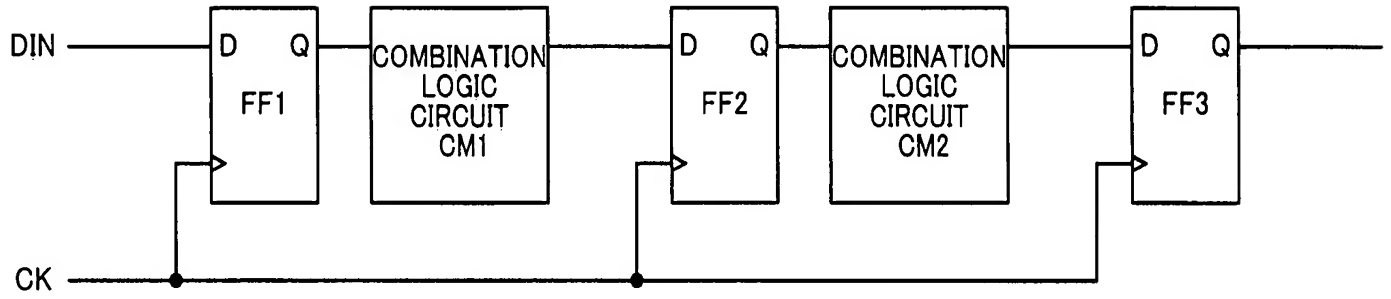

DIN
D
Q
FF1
COMBINATION LOGIC CIRCUIT CM1
D
Q
FF2
COMBINATION LOGIC CIRCUIT CM2
D
Q
FF3
CK

FIG. 9B

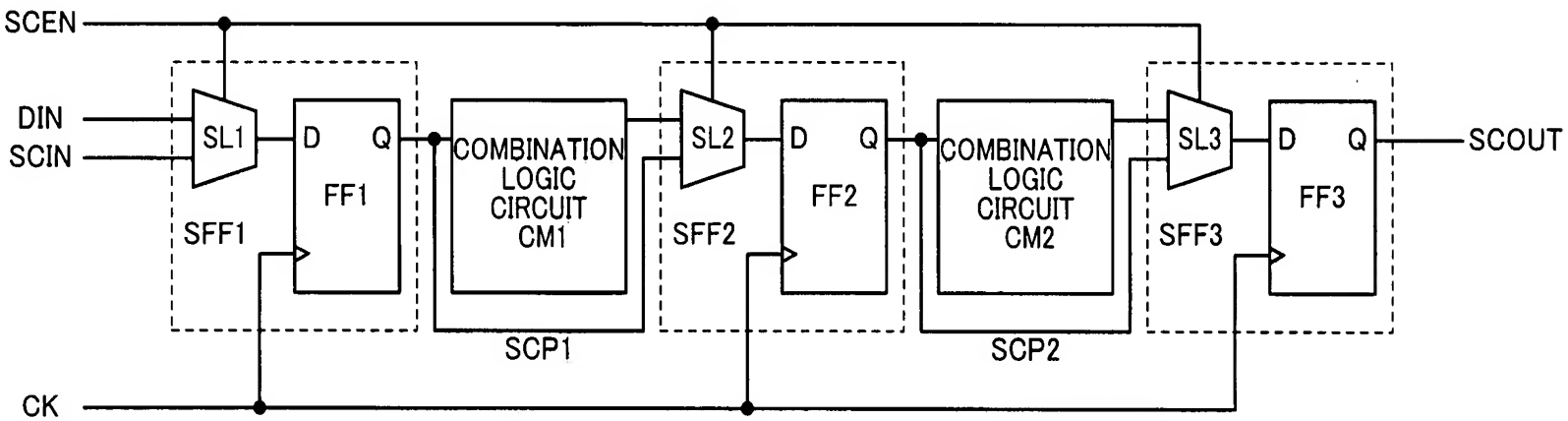

SCEN
DIN
SCIN
SL1
D
Q
FF1
SFF1
COMBINATION LOGIC CIRCUIT CM1
SCP1
SL2
D
Q
FF2
SFF2
COMBINATION LOGIC CIRCUIT CM2
SCP2
SL3
D
Q
FF3
SFF3
SCOUT
CK

FIG. 10

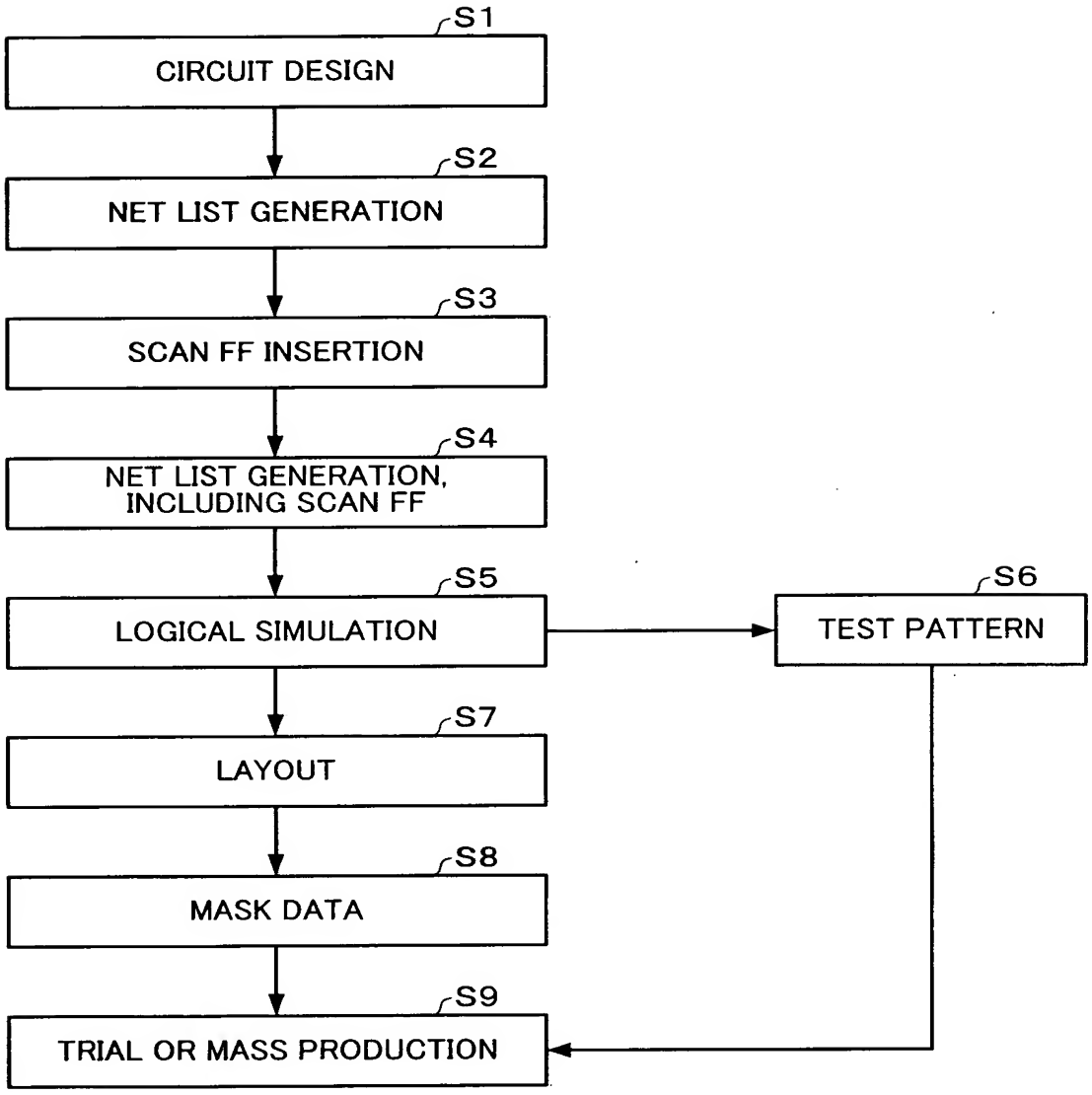

S1
CIRCUIT DESIGN
S2
NET LIST GENERATION
S3
SCAN FF INSERTION
S4
NET LIST GENERATION, INCLUDING SCAN FF
S5
LOGICAL SIMULATION
S6
TEST PATTERN
S7
LAYOUT
S8
MASK DATA
S9
TRIAL OR MASS PRODUCTION

FIG. 11

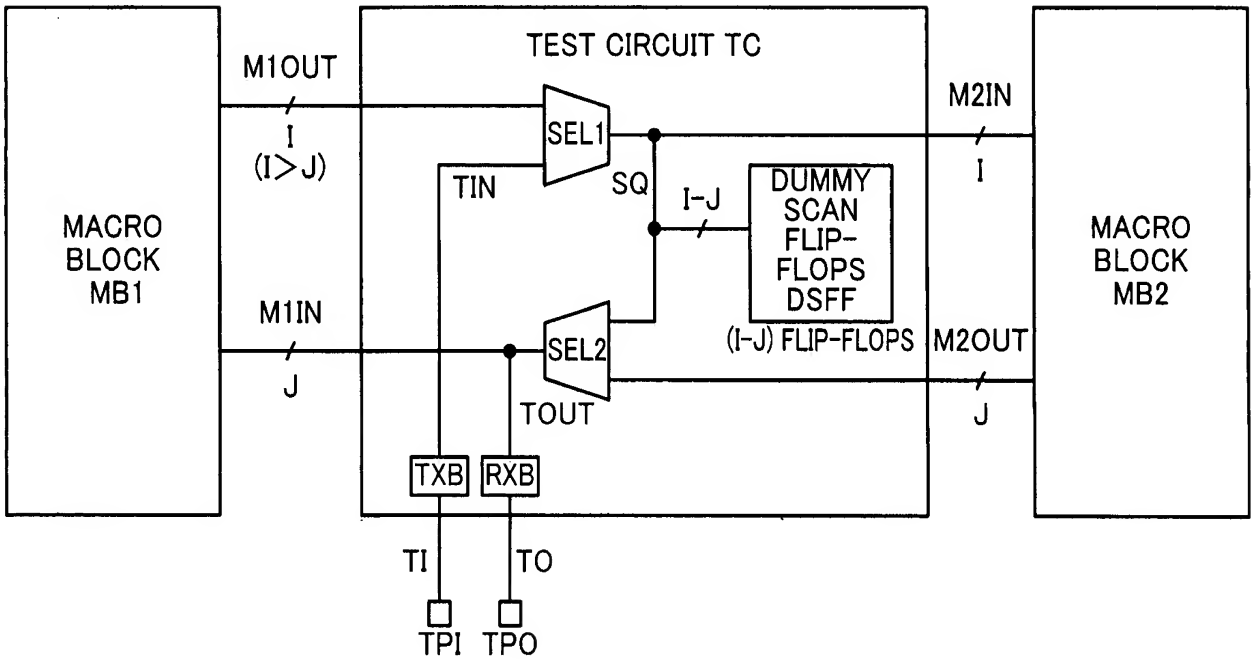

MACRO BLOCK MB1
M1OUT
I
(I>J)
M1IN
J
TEST CIRCUIT TC
SEL1
SEL2
TIN
SQ
I-J
DUMMY SCAN FLIP-FLOPS DSFF
(I-J) FLIP-FLOPS
TOUT
TXB
RXB
TI
TO
TPI
TPO
M2IN
I
M2OUT
J
MACRO BLOCK MB2

FIG. 12A

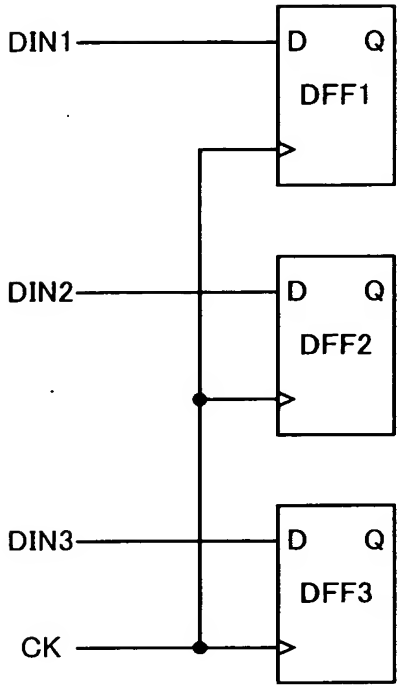


FIG. 12B

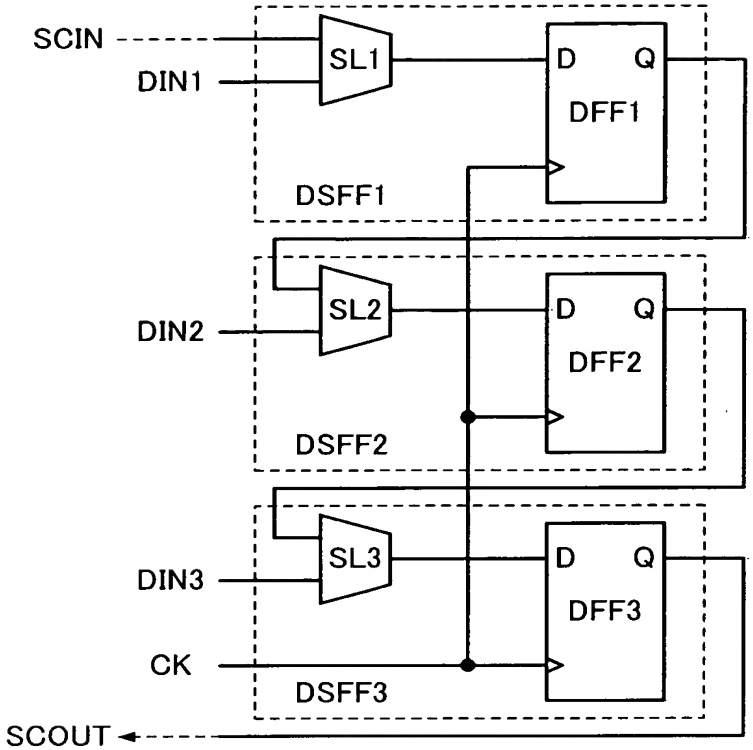


FIG. 12C

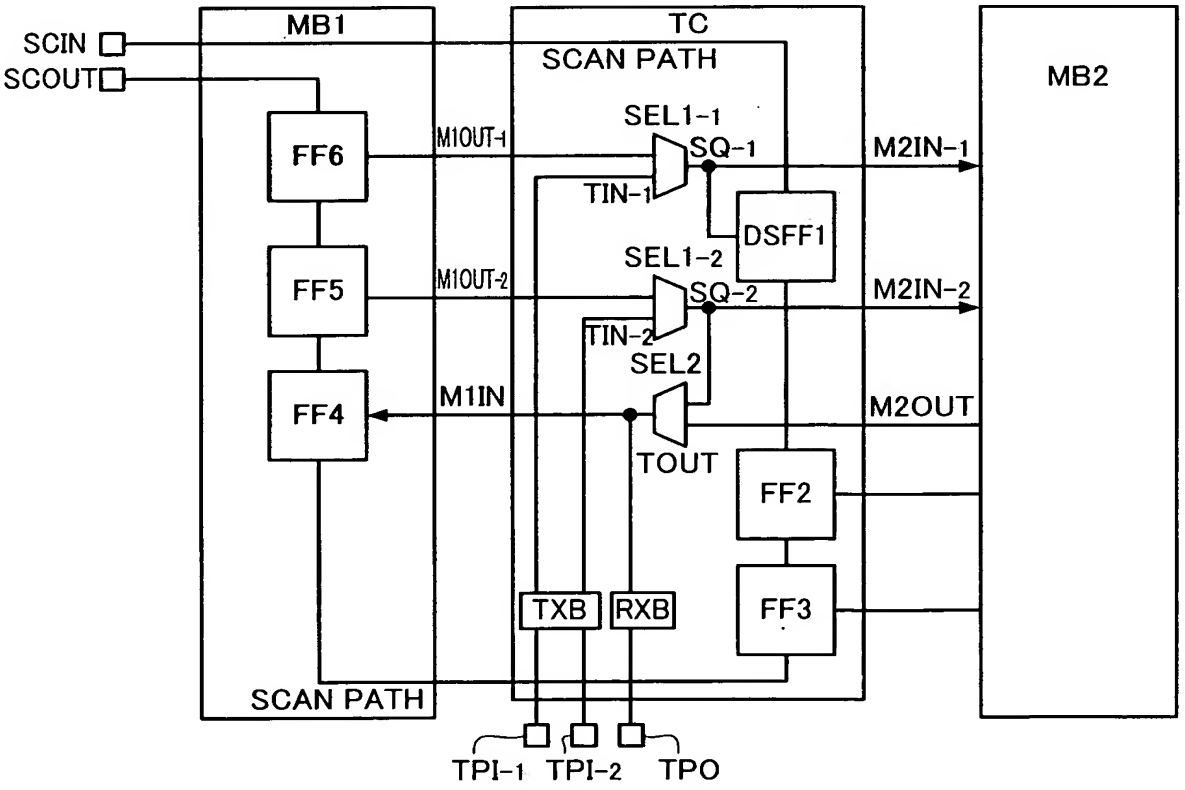


FIG. 13

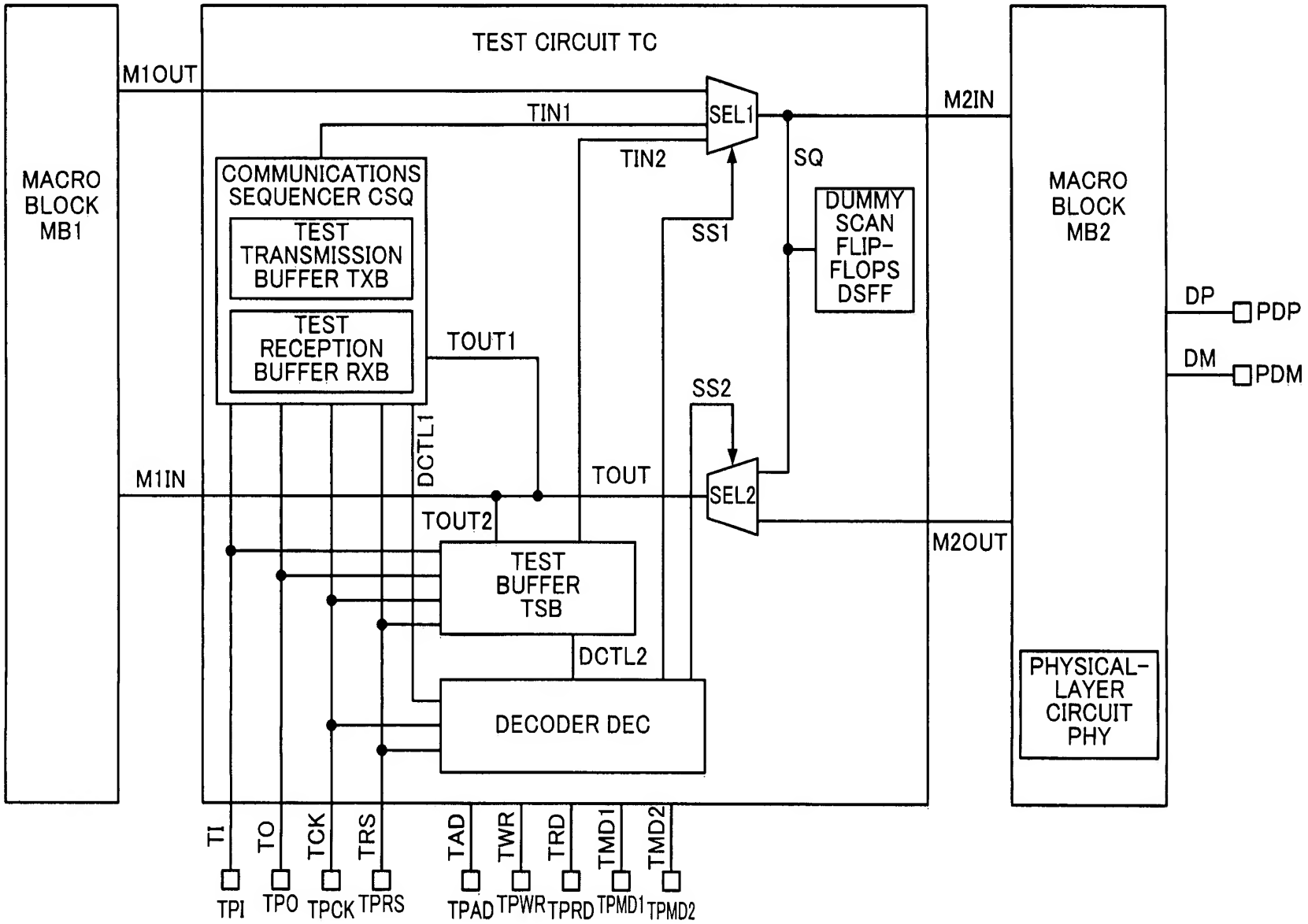

TEST CIRCUIT TC
MACRO BLOCK MB1
M1OUT
TIN1
SEL1
M2IN
TIN2
SQ
COMMUNICATIONS SEQUENCER CSQ
TEST TRANSMISSION BUFFER TXB
TEST RECEPTION BUFFER RXB
SS1
DUMMY SCAN FLIP-FLOPS DSFF
MACRO BLOCK MB2
DP
PDP
DM
PDM
TOUT1
SS2
DCTL1
M1IN
TOUT
SEL2
TOUT2
M2OUT
TEST BUFFER TSB
DCTL2
PHYSICAL-LAYER CIRCUIT PHY
DECODER DEC
TI
TO
TCK
TRS
TAD
TWR
TRD
TMD1
TMD2
TPI
TPO
TPCK
TPRS
TPAD
TPWR
TPRD
TPMD1
TPMD2

FIG. 14

TAD	TRD/TWR	Bit3	Bit2	Bit1	Bit0
0x0	W	TxBuf0[7]	TxBuf0[6]	TxBuf0[5]	TxBuf0[4]
0x0	R	RxBuf0[7]	RxBuf0[6]	RxBuf0[5]	RxBuf0[4]
0x1	W	TxBuf0[3]	TxBuf0[2]	TxBuf0[1]	TxBuf0[0]
0x1	R	RxBuf0[3]	RxBuf0[2]	RxBuf0[1]	RxBuf0[0]
0x2	W	TxBuf1[7]	TxBuf1[6]	TxBuf1[5]	TxBuf1[4]
0x2	R	RxBuf1[7]	RxBuf1[6]	RxBuf1[5]	RxBuf1[4]
0x3	W	TxBuf1[3]	TxBuf1[2]	TxBuf1[1]	TxBuf1[0]
0x3	R	RxBuf1[3]	RxBuf1[2]	RxBuf1[1]	RxBuf1[0]
0x4	W	TxBuf2[7]	TxBuf2[6]	TxBuf2[5]	TxBuf2[4]
0x4	R	RxBuf2[7]	RxBuf2[6]	RxBuf2[5]	RxBuf2[4]
0x5	W	TxBuf2[3]	TxBuf2[2]	TxBuf2[1]	TxBuf2[0]
0x5	R	RxBuf2[3]	RxBuf2[2]	RxBuf2[1]	RxBuf2[0]
0x6	W	TxBuf3[7]	TxBuf3[6]	TxBuf3[5]	TxBuf3[4]
0x6	R	RxBuf3[7]	RxBuf3[6]	RxBuf3[5]	RxBuf3[4]
0x7	W	TxBuf3[3]	TxBuf3[2]	TxBuf3[1]	TxBuf3[0]
0x7	R	RxBuf3[3]	RxBuf3[2]	RxBuf3[1]	RxBuf3[0]
0x8	R/W	–	–	TXMODE	–
0x9	R/W	XCVRSELECT	TERMSELECT	OPMODE1	OPMODE0
0xA	R/W	PLLSELECT	OSCENB	CLKSELECT1	CLKSELECT0
0xB	R/W	RESET	RAWCLOCK	ANA_IQ	SUSPEND
0xC	R/W	OPENLOOP	TglCLK	DivideCLK	MonCLK(R)
0xD	R	MonRXACTIVE	MonRXERROR	MonLINESTATE1	MonLINESTATE0
0xE	R/W	–	–	MonRXERROR(R)	LatRXERROR
0xF	R/W	–	–	–	TXSTART

FIG. 15A

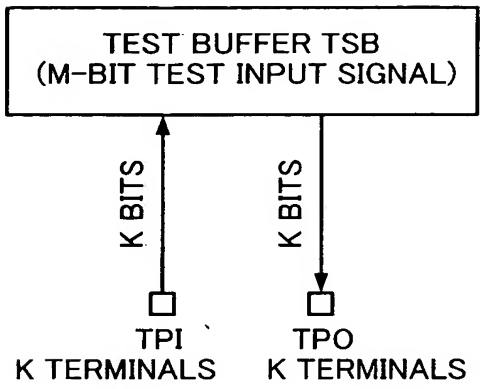


FIG. 15B

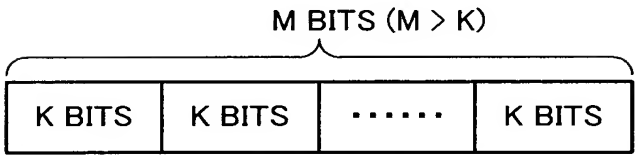


FIG. 15C

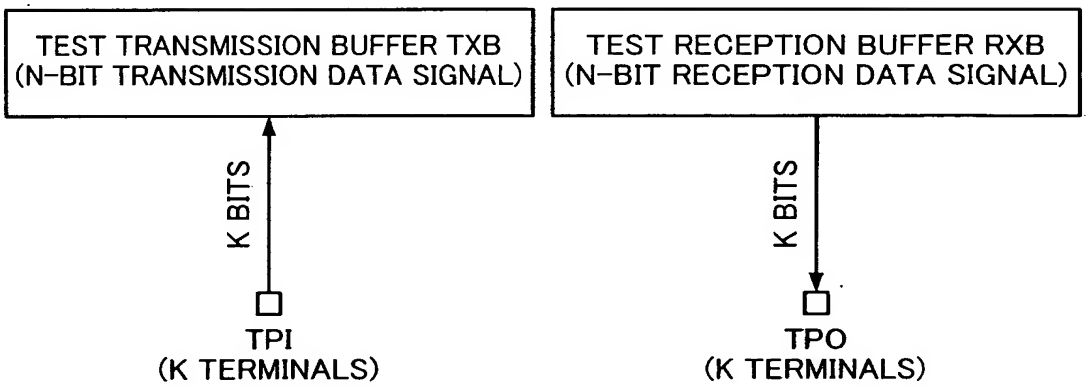


FIG. 15D

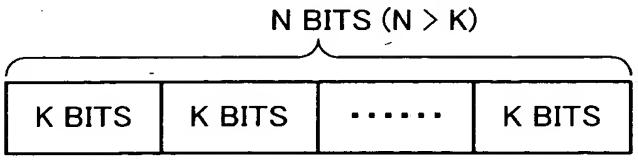


FIG. 16

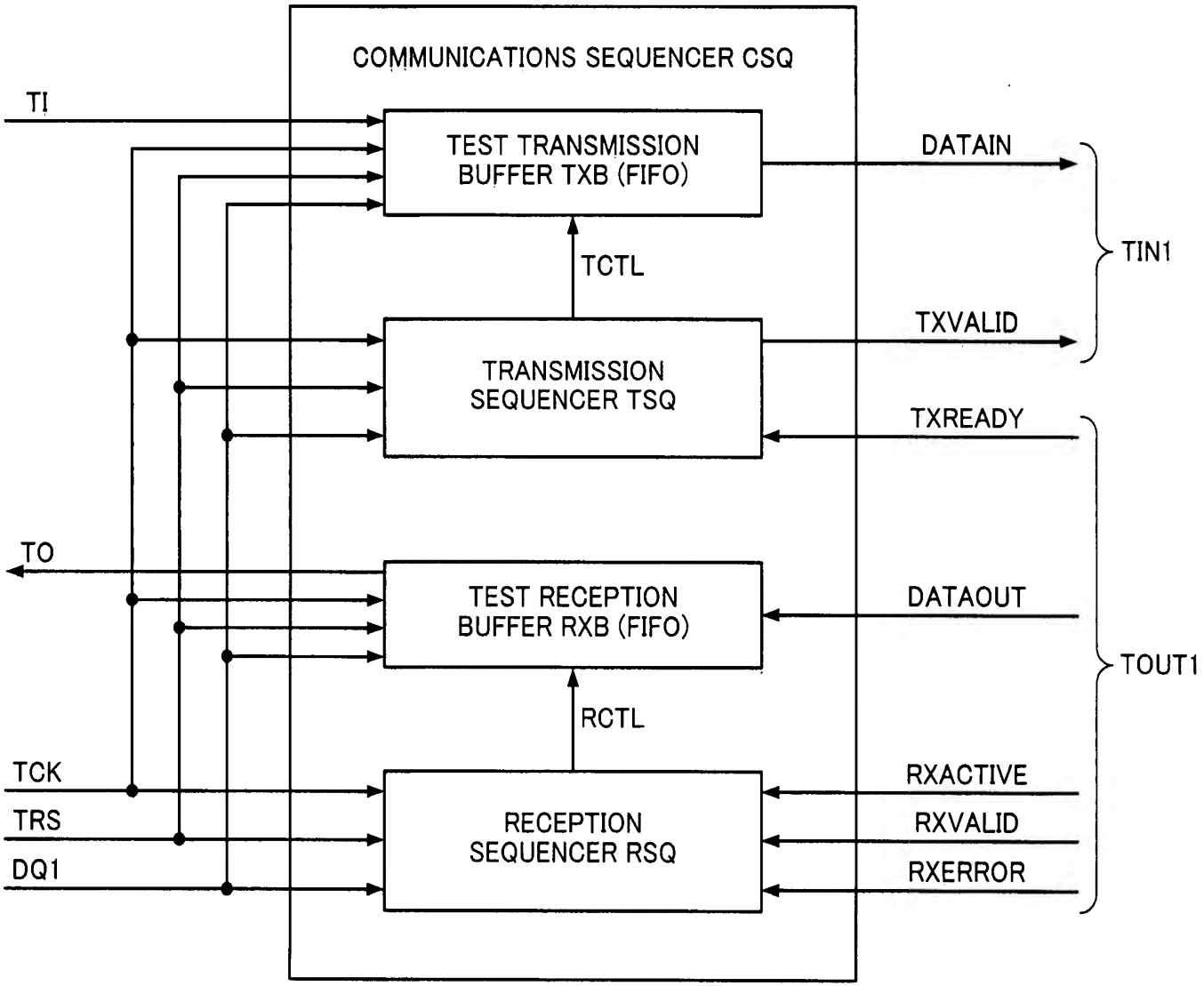

COMMUNICATIONS SEQUENCER CSQ
TI
TEST TRANSMISSION BUFFER TXB (FIFO)
DATAIN
TCTL
TXVALID
TIN1
TRANSMISSION SEQUENCER TSQ
TXREADY
TO
TEST RECEPTION BUFFER RXB (FIFO)
DATAOUT
TOUT1
RCTL
TCK
TRS
DQ1
RECEPTION SEQUENCER RSQ
RXACTIVE
RXVALID
RXERROR

FIG. 17

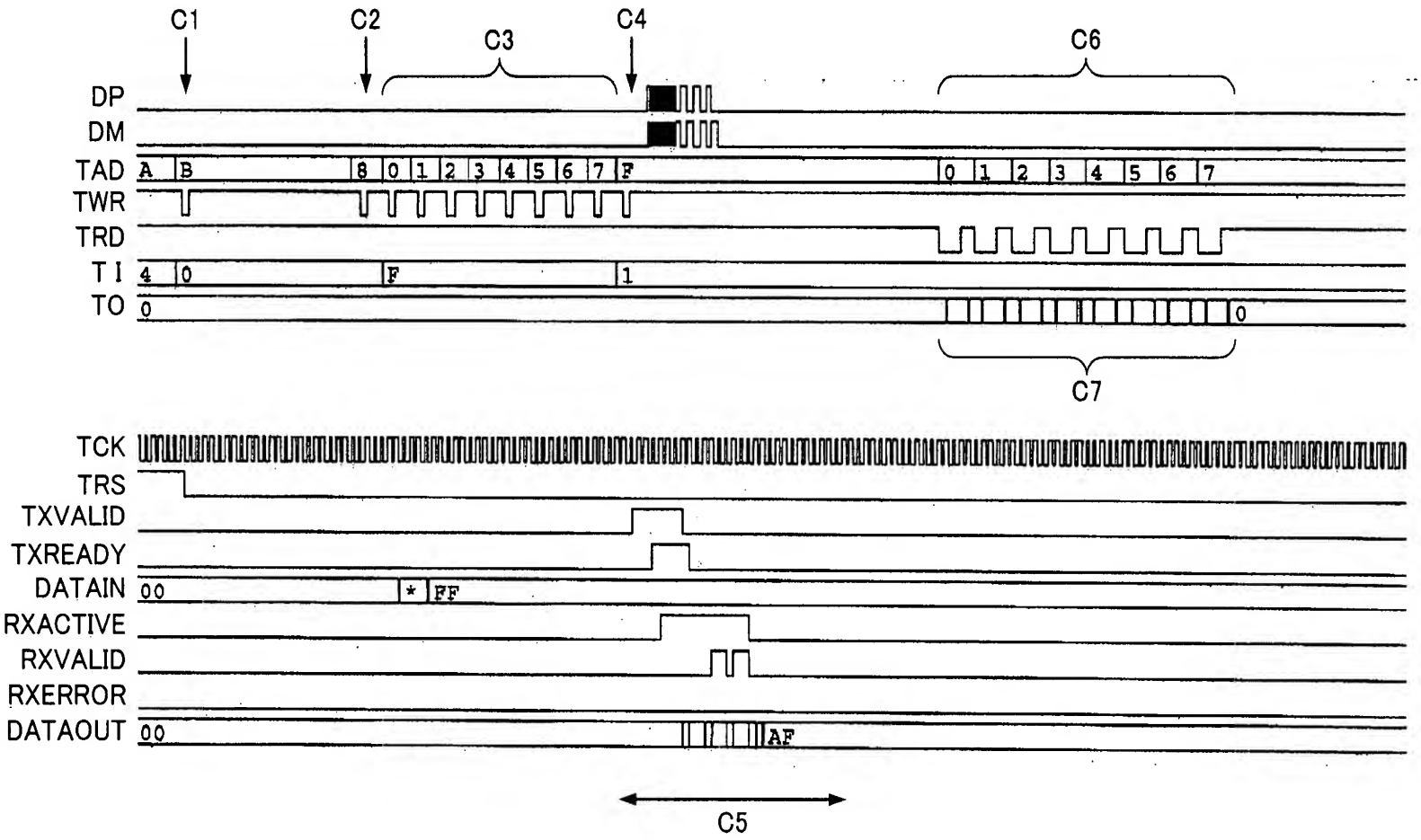

C1
C2
C3
C4
C6
C7
C5
DP
DM
TAD
TWR
TRD
T I
TO
TCK
TRS
TXVALID
TXREADY
DATAIN
RXACTIVE
RXVALID
RXERROR
DATAOUT
A B 8 0 1 2 3 4 5 6 7 F
0 1 2 3 4 5 6 7
4 0
F
1
0
0
00
*
FF
00
AF

FIG. 18

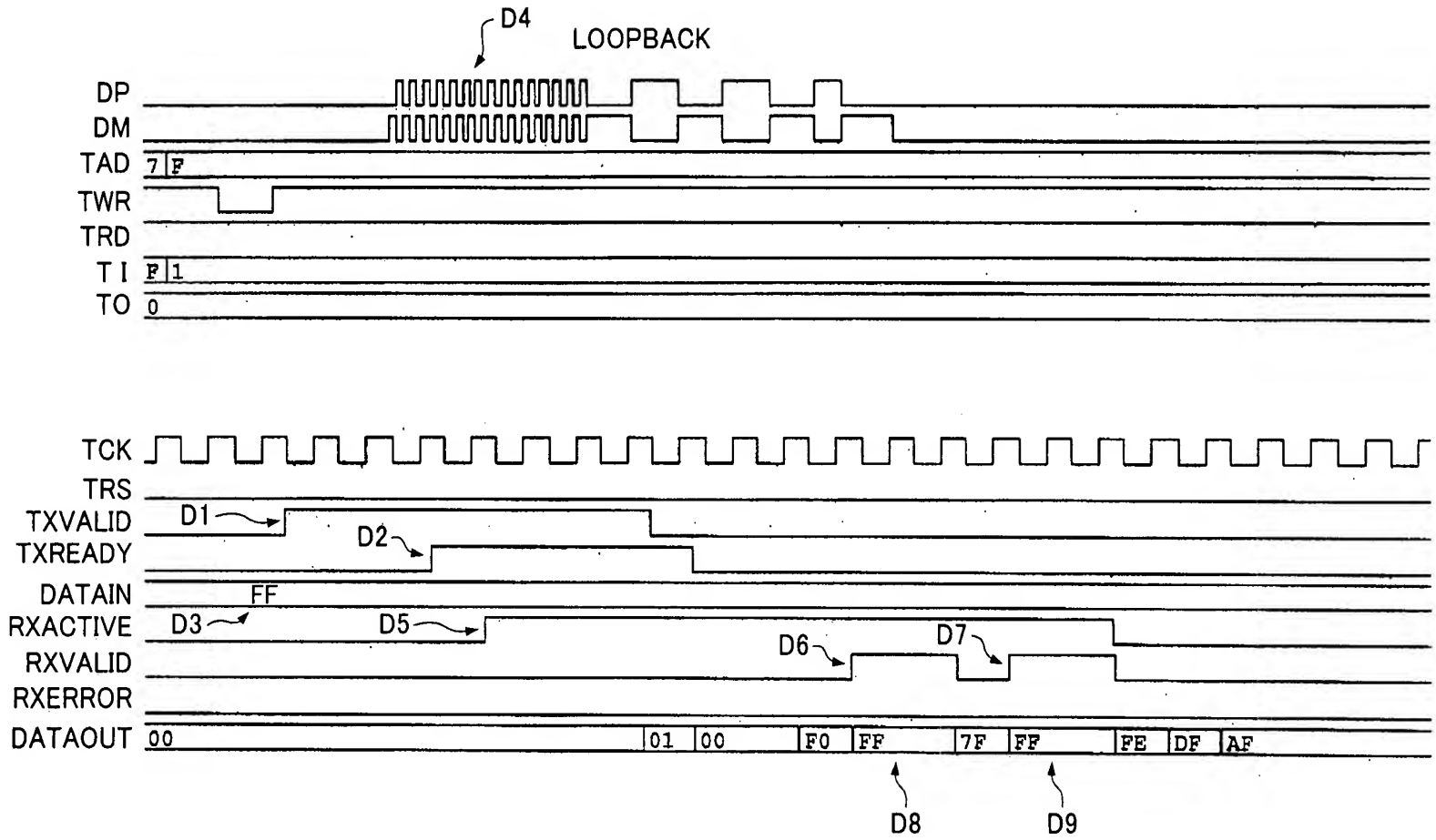

D4
LOOPBACK
DP
DM
TAD
7
F
TWR
TRD
TI
F
1
TO
0
TCK
TRS
TXVALID
D1
D2
TXREADY
DATAIN
FF
RXACTIVE
D3
D5
D6
D7
RXVALID
RXERROR
DATAOUT
00
01
00
F0
FF
7F
FF
FE
DF
AF
D8
D9

FIG. 19

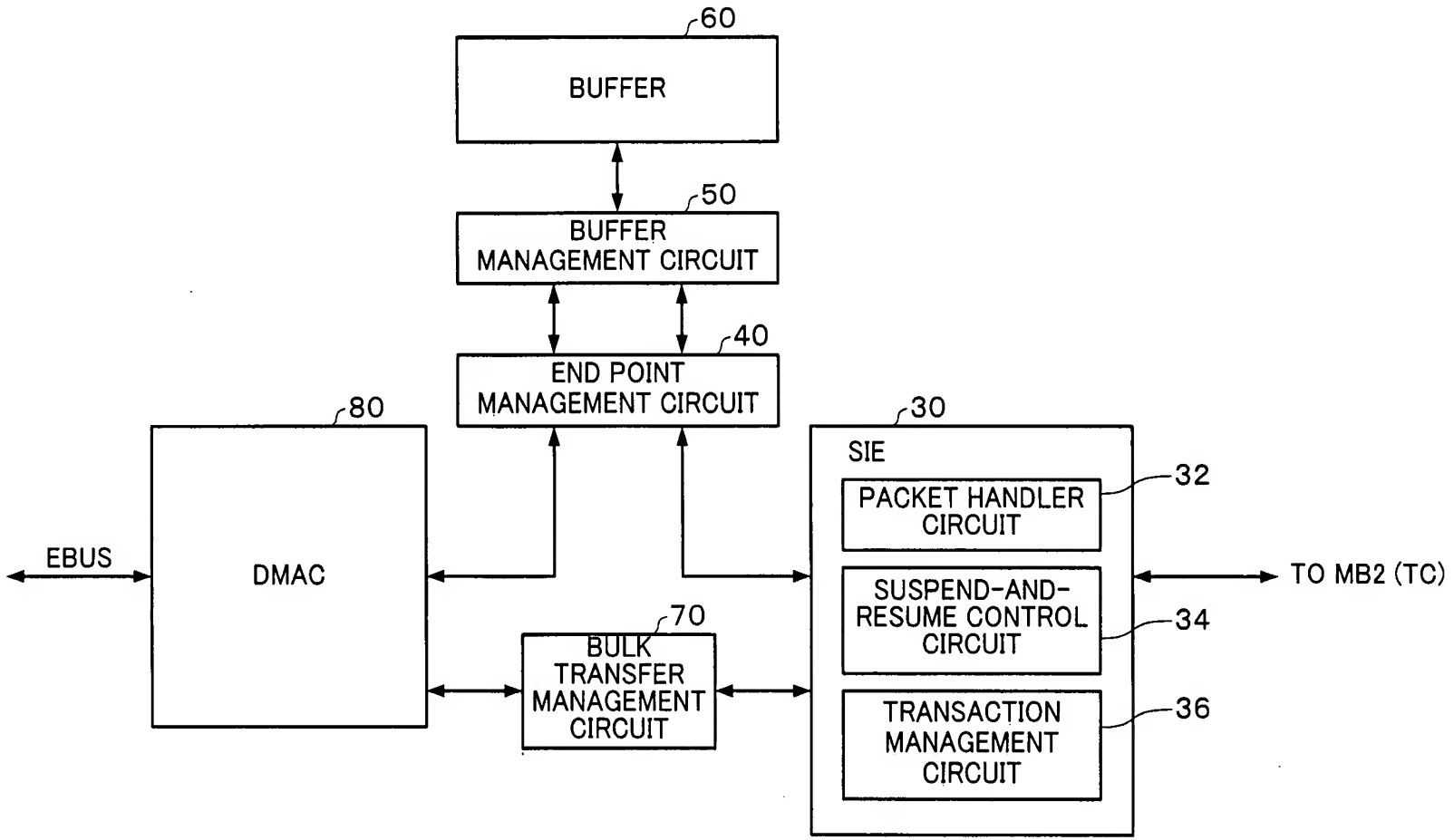
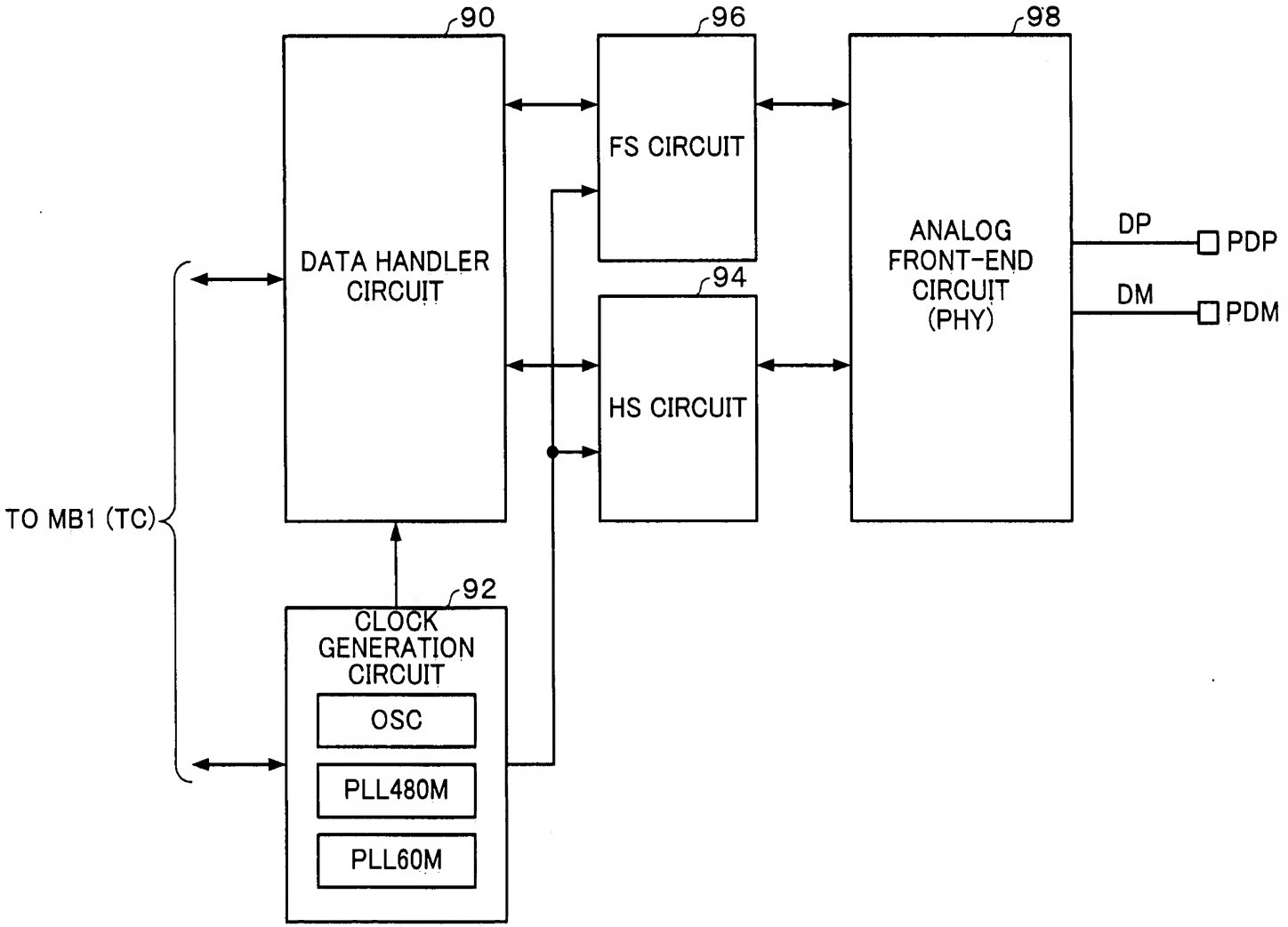

60
BUFFER
50
BUFFER MANAGEMENT CIRCUIT
40
END POINT MANAGEMENT CIRCUIT
80
DMAC
EBUS
70
BULK TRANSFER MANAGEMENT CIRCUIT
30
SIE
PACKET HANDLER CIRCUIT
32
SUSPEND-AND-RESUME CONTROL CIRCUIT
34
TRANSACTION MANAGEMENT CIRCUIT
36
TO MB2 (TC)

FIG. 20


90
96
98
FS CIRCUIT
DATA HANDLER CIRCUIT
ANALOG FRONT-END CIRCUIT (PHY)
DP
PDP
DM
PDM
94
HS CIRCUIT
TO MB1 (TC)
92
CLOCK GENERATION CIRCUIT
OSC
PLL480M
PLL60M